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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 27

Application Number: 09/461,643
Filing Date: December 14, 1999
Appellant(s): DOW, KEITH

John F. Conroy (Reg. No. 45,485)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 15th of March 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that the claim group I (i.e., claims 1, 3-8, 10-14, 16-20, 23 and 24), the claim group II (i.e., claims 8 and 10-13) and the claim group III (i.e., claims 14 and 16-19) do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

AAPA	Applicant's Admitted Prior Art in the Applicant's Background Disclosure	
US 6,160,716 A	Perino et al.	12-2000

US 4,904,968 Theus 02-1990

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 4-8, 11-14, 16-20, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art [hereinafter AAPA] in view of Perino et al. [US 6,160,716 A; hereinafter Perino].

Referring to claim 1, AAPA discloses a computer system 100 (Fig. 1) comprising: processor (i.e., CPU 105 of Fig. 1); a memory unit (i.e., memory hub 110 of Fig. 1) configuring to store data used by said processor (See Fig. 1 and page 1, lines 10-13; i.e., wherein in fact that the computer including CPU, memory unit, MCU, and MCU controlling the flow of data into and out of memory unit implies said memory unit configuring to store data used by said processor); a memory control unit (i.e., memory control unit 120 of Fig. 1) configured to manage data flowing into and out of said memory unit (See page 1, lines 12-13); and a circuit board (See Fig. 1 and Fig. 2; i.e., in fact, all the components within said computer systems are fabricated on a circuit board, which is well known to one of ordinary skill in the art of personal computer system at the time the invention was made. Especially, AAPA teaches a part of circuit board routing geometry between said MCU and said memory unit, as shown in Fig. 2) comprising: a first signal line (i.e., signal line 150 of Fig. 2), formed on a first layer of said circuit board (e.g., surface layer on said circuit board) and connected between a first pin (i.e., pin 155 of Fig. 2) on said memory unit and said memory control unit (See page 2, lines 3-8); and a second signal line (i.e., signal line 160 of Fig. 2) also formed on said first layer (e.g., said surface layer on said circuit board) of said circuit board and connected to said first pin on said memory unit (See page 2, lines 8-10), a first portion of said second signal line (i.e., "neck down" portion of signal line 160 of Fig. 2) at an acute angle (i.e., angle between neck down portions of the first and second signal lines in Fig. 2; Note the definition of the term "acute" in

dictionary states "ending in a sharp point: as being or forming an angle measuring less than 90 degrees", Merriam Webster's Collegiate Dictionary by Merriam-Webster, Inc.") relative to a first portion of said first signal line (i.e., "neck down" portion of signal line 150 of Fig. 2).

AAPA does not teach said circuit board comprising a second portion of said second signal line substantially parallel to a second portion of said first signal line; at least two layers formed in parallel to a surface of said circuit board, and wherein said first layer defines a non-grounded gap between said first and second portions of said first and second signal lines.

Perino discloses a circuit board (i.e., motherboard 110 of Fig. 1) comprising a second portion of a second signal line (e.g., a second half of trace 870 of Fig. 8, Example B) substantially parallel to a second portion of a first signal line (e.g., a second half of trace 880 of Fig. 8, Example B) with having substantially equal widths of said signal lines, and a distance (i.e., space) between said signal lines (i.e., 8 mils signal line in Fig. 8, Example B); at least two layers (e.g., signal traces' plane and a ground plane) formed in parallel to a surface (i.e., surface for the signal traces and pad contacts 1420 of Fig. 14) of said circuit board (See col. 4, lines 62-67), and wherein a layer (i.e., surface layer of motherboard 110 of Fig. 1) defines a non-grounded gap between a first portion and second portion of said first and second signal lines (i.e., a first and second half of respective traces 870 and 880 in Fig. 8, Example B; See Figs. 8 and 16, See col. 4, lines 66-67 and col. 7, lines 21-26; i.e., wherein in fact that a ground plane is on the backside of the motherboard, and those figures implies that a ground gap is not between said first portion and second portion of said first and second signal lines). Further, Perino suggests to the artisan to place, or not to place a ground gap between said signal lines (i.e., signal traces) based upon the need for signal isolation between said signal lines, i.e., (1) placement of large spacing without needing said ground gap, (2) providing said ground gap between said signal lines for preventing signal interferences, or (3) said ground gap may be selectively used between said signal lines that may cause interferences (See col. 5, line 56-58, col. 6, lines 14-17 and 36-38). In fact, AAPA teaches said signal lines are connected at said first pin (i.e.,

constructing one single connection line), thus the artisan does not place said ground gap (i.e., ground tracer) between said signal lines according to Perino's clear suggestion because said signal lines (i.e., one single connection line) doesn't cause any interferences (See col. 6, lines 36-38 about said ground gap may be selectively used between said signal lines that may cause interferences).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have motivated to employ the concept of the line width and space determination, as disclosed by Perino, to said circuit board routing, as disclosed by AAPA, so as to make (1) a second portion of said first signal line and a second portion of said second signal line route with a separating distance, and (2) said signal line widths of said first and second signal lines are equal to the width of said separating distance for the determined impedance values, for the advantage of eliminating reflected signals and signal deterioration caused by a mismatched impedance (See Perino, col. 5 lines 29-32).

Referring to claim 4, Perino teaches said second portion of said first signal line (i.e., a second half of trace 880 of Fig. 8, Example B) and said second portion of said second signal line (i.e., a second half of trace 870 of Fig. 8, Example B) have substantially equal widths (i.e., 8 mils signal line in Fig. 8, Example B).

Referring to claim 5, Perino teaches said second portion of said first signal line (i.e., a second half of trace 880 of Fig. 8, Example B) and said second portion of said second signal line (i.e., a second half of trace 870 of Fig. 8, Example B) are separated by a perpendicular distance (i.e., a right angle distance with two signal lines, such as the shortest distance, 8 mils space in Fig. 8, Example B) substantially equal to said widths (i.e., 8 mils signal line in Fig. 8, Example B).

Referring to claim 6, AAPA, as modified by Perino, discloses all the limitations of the claim 6 including said width of said lines are each substantially equal to 5 mils (See AAPA, page 2, lines 7-9) except that does not teach said perpendicular distance separating said second portion of said lines are each substantially equal to 5 mils.

However, the claim 6 recites the subject matter "the perpendicular distance separating the second portion of the lines are each substantially equal to 5 mils" without any patentable advantage in the specification (See the claim 6 and amended specification (filed on 14th of August, 2002) page 2, lines 8-20), such as the reason of substantially equal to 5 mils rather than 8 mils with any patentable advantage. Therefore, the subject matter "substantially equal to 5 mils" in the claim is not patentably significant since it at most relates to the width of space between said signal lines under consideration which is not ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.*

Referring to claim 7, AAPA disclose said memory unit is a Rambus device (See page 1, line 19 through page 2, line 2).

Referring to claim 8, AAPA discloses a method for use in routing signals between a memory unit and a memory control unit (See Fig. 1 and page 1, lines 10-13; i.e., wherein in fact that the computer including CPU, memory unit, MCU, and MCU controlling the flow of data into and out of memory unit implies a method for use in routing signals between a memory unit and a memory control unit), said method comprising: delivering a first signal over a first signal line (i.e., signal over signal line 150 of Fig. 2) formed on a first layer of a multi-layer circuit board (e.g., surface layer on multi-layer circuit board; See page 2, lines 11-15, wherein in fact that "...formed on different layers of the circuit board..." clearly teaches that a circuit board is a multi-layer circuit board) and connected between said memory control unit and a first pin (i.e., pin 155 of Fig. 2) on said memory unit (See page 2, lines 3-8); delivering a second signal over a second signal line (i.e., signal over signal line 160 of Fig. 2) formed on said first layer (e.g., said surface layer on said circuit board) of said circuit board and connected to said first pin on said memory unit (See page 2, lines 8-10), a first portion of said second signal line (i.e., "neck down" portion of signal line 160 of Fig. 2) formed at an acute angle (i.e., angle between neck down portions of the first and second signal lines in Fig. 2; Note the definition of the term "acute" in dictionary states "ending in a sharp point: as being or forming an angle measuring less than 90 degrees", Merriam

Webster's Collegiate Dictionary by Merriam-Webster, Inc.") relative to a first portion of said first signal line (i.e., "neck down" portion of signal line 150 of Fig. 2).

AAPA does not expressly teach said multi-layer circuit board comprising: said first layer being formed in parallel to a second layer on said surface of said multi-layer circuit board; a second portion of said second signal line formed substantially parallel to a second portion of said first signal line; and said first and second portions of said first and second signal lines separated without a ground connection therebetween. Perino discloses a circuit board (i.e., motherboard 110 of Fig. 1), wherein a first layer (e.g., signal traces' plane) being formed in parallel to a second layer (i.e., a ground plane) on a surface (i.e., surface for the signal traces and pad contacts 1420 of Fig. 14) of a multi-layer circuit board (See col. 4, lines 62-67); a second portion of a second signal line (e.g., a second half of trace 870 of Fig. 8, Example B) formed substantially parallel to a second portion of a first signal line (e.g., a second half of trace 880 of Fig. 8, Example B) with having substantially equal widths of said signal lines, and a distance (i.e., space) between said signal lines (i.e., 8 mils signal line in Fig. 8, Example B); and said first and second portions of said first and second signal lines separated without a ground connection therebetween (i.e., a first and second half of respective traces 870 and 880 in Fig. 8, Example B; See Figs. 8 and 16, See col. 4, lines 66-67 and col. 7, lines 21-26; i.e., wherein in fact that a ground plane is on the backside of the motherboard, and those figures implies that a ground gap is not between said first portion and second portion of said first and second signal lines). Further, Perino suggests to the artisan to place, or not to place a ground connection between said signal lines (i.e., signal traces) based upon the need for signal isolation between said signal lines, i.e., (1) placement of large spacing without needing said ground connection, (2) providing said ground connection between said signal lines for preventing signal interferences, or (3) said ground connection may be selectively used between said signal lines that may cause interferences (See col. 5, line 56-58, col. 6, lines 14-17 and 36-38). In fact, AAPA teaches said signal lines are connected at said first pin (i.e., constructing one single connection line), thus the artisan

does not place said ground connection (i.e., ground tracer) between said signal lines according to Perino's clear suggestion because said signal lines (i.e., one single connection line) doesn't cause any interferences (See col. 6, lines 36-38 about said ground connection may be selectively used between said signal lines that may cause interferences).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have motivated to employ the concept of the line width and space determination, as disclosed by Perino, to said method for said circuit board routing, as disclosed by AAPA, so as to make (1) a second portion of said first signal line and a second portion of said second signal line route with a separating distance, and (2) said signal line widths of said first and second signal lines are equal to the width of said separating distance for the determined impedance values, for the advantage of eliminating reflected signals and signal deterioration caused by a mismatched impedance (See Perino, col. 5 lines 29-32).

Referring to claim 11, Perino teaches delivering said first signal and said second signal (i.e., signals on the respective traces 870 and 880 in Fig. 8, Example B) includes delivering said signals over second portions of said first and second signal lines (i.e., said signals on the respective second halves of traces 870 and 880 in Fig. 8, Example B) that have substantially equal widths (i.e., 8 mils signal line in Fig. 8, Example B).

Referring to claim 12, Perino teaches delivering said first signal and said second signal (i.e., signals on the respective traces 870 and 880 in Fig. 8, Example B) includes delivering said signals over second portions of said first and second signal lines (i.e., said signals on the respective second halves of traces 870 and 880 in Fig. 8, Example B) that are separated by a perpendicular distance (i.e., a right angle distance with two signal lines, such as the shortest distance, 8 mils space in Fig. 8, Example B) substantially equal to their widths (i.e., 8 mils signal line in Fig. 8, Example B).

Referring to claim 13, AAPA, as modified by Perino, discloses all the limitations of the claim 13 including said width of said lines are each substantially equal to 5 mils (See AAPA, page 2, lines 7-9)

except that does not teach said perpendicular distance separating said second portion of said lines are each substantially equal to 5 mils.

However, the claim 13 recites the subject matter "being separated by a perpendicular distance substantially equal to 5 mils" without any patentable advantage in the specification (See the claim 13 and amended specification (filed on 14th of August, 2002) page 2, lines 8-20), such as the reason of substantially equal to 5 mils rather than 8 mils with any patentable advantage. Therefore, the subject matter "substantially equal to 5 mils" in the claim is not patentably significant since it at most relates to the width of space between said signal lines under consideration which is not ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.*

Referring to claim 14, AAPA discloses a method for use in manufacturing a computer system 100 (Fig. 1) comprising: forming first and second signal lines (i.e., signal lines 150 and 160 in Fig. 2) on a first layer of a circuit board (e.g., surface layer on a circuit board; See Fig. 1 and Fig. 2; i.e., in fact, all the components within said computer systems are fabricated on a circuit board, which is well known to one of ordinary skill in the art of personal computer system at the time the invention was made. Especially, AAPA teaches a part of circuit board routing geometry between said MCU and said memory unit, as shown in Fig. 2); connecting a memory unit (i.e., memory hub 110 of Fig. 1) to said board such that a first pin (i.e., pin 155 of Fig. 2) on said memory unit connects to said first and second signal lines (i.e., signal lines 150 and 160 in Fig. 2); affixing a memory control unit (i.e., memory control unit 120 of Fig. 1) to said board such that said memory control unit connects to at least said first signal line (See page 2, lines 3-8); forming a first portion of said second signal line (i.e., "neck down" portion of signal line 160 of Fig. 2) to be at an acute angle (i.e., angle between neck down portions of the first and second signal lines in Fig. 2; Note the definition of the term "acute" in dictionary states "ending in a sharp point: as being or forming an angle measuring less than 90 degrees", Merriam Webster's Collegiate Dictionary by Merriam-

Webster, Inc.") relative to a first portion of said first signal line (i.e., "neck down" portion of signal line 150 of Fig. 2).

AAPA does not teach said method comprising forming at least two layers parallel to a surface of a circuit board; forming a second portion of said second signal line to be substantially parallel to a second portion of said first signal line.

Perino discloses a circuit board (i.e., motherboard 110 of Fig. 1), wherein at least two layers (e.g., signal traces' plane and a ground plane) formed in parallel to a surface (i.e., surface for the signal traces and pad contacts 1420 of Fig. 14) of said circuit board (See col. 4, lines 62-67); a second portion of a second signal line (e.g., a second half of trace 870 of Fig. 8, Example B) to be substantially parallel to a second portion of a first signal line (e.g., a second half of trace 880 of Fig. 8, Example B) with having substantially equal widths of said signal lines, and a distance (i.e., space) between said signal lines (i.e., 8 mils signal line in Fig. 8, Example B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have motivated to employ the concept of the line width and space determination, as disclosed by Perino, to said method of circuit board routing, as disclosed by AAPA, so as to make (1) a second portion of said first signal line and a second portion of said second signal line route with a separating distance, and (2) said signal line widths of said first and second signal lines are equal to the width of said separating distance for the determined impedance values, for the advantage of eliminating reflected signals and signal deterioration caused by a mismatched impedance (See Perino, col. 5 lines 29-32).

Referring to claim 16, Perino teaches forming said first and second signal lines such that no conductive trace (e.g., any trace) lies between a first portion and second portion of said first and second signal lines (i.e., a first and second half of respective traces 870 and 880 in Fig. 8, Example B; See Figs. 8 and 16, i.e., no conductor line between traces 870 and 880 in Fig. 8 for maintaining the same width and space).

Referring to claim 17, Perino teaches forming said second portion of said first signal line (i.e., a second half of trace 880 of Fig. 8, Example B) and said second portion of said second signal line (i.e., a second half of trace 870 of Fig. 8, Example B) to have substantially equal widths (i.e., 8 mils signal line in Fig. 8, Example B).

Referring to claim 18, Perino teaches forming said second portion of said first signal line (i.e., a second half of trace 880 of Fig. 8, Example B) and said second portion of said second signal line (i.e., a second half of trace 870 of Fig. 8, Example B) to be separated by a perpendicular distance (i.e., a right angle distance with two signal lines, such as the shortest distance, 8 mils space in Fig. 8, Example B) substantially equal to their widths (i.e., 8 mils signal line in Fig. 8, Example B).

Referring to claim 19, AAPA, as modified by Perino, discloses all the limitations of the claim 19 including said width of said lines are each substantially equal to 5 mils (See AAPA, page 2, lines 7-9) except that does not teach said perpendicular distance separating said second portion of said lines are each substantially equal to 5 mils.

However, the claim 19 recites the subject matter "the perpendicular distance separating the second portion of the lines are each substantially equal to 5 mils" without any patentable advantage in the specification (See the claim 19 and amended specification (filed on 14th of August, 2002) page 2, lines 8-20), such as the reason of substantially equal to 5 mils rather than 8 mils with any patentable advantage. Therefore, the subject matter "substantially equal to 5 mils" in the claim is not patentably significant since it at most relates to the width of space between said signal lines under consideration which is not ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.*

Referring to claim 20, AAPA discloses a circuit board (See Fig. 1 and Fig. 2; i.e., in fact, all the components within said computer systems are fabricated on a circuit board, which is well known to one of ordinary skill in the art of personal computer system at the time the invention was made. Especially, AAPA teaches a part of circuit board routing geometry between said MCU and said memory unit, as

shown in Fig. 2) for use in a computer system (Fig. 1) comprising: a memory unit (i.e., memory hub 110 of Fig. 1); a memory control unit (i.e., memory control unit 120 of Fig. 1); and a data bus connecting said memory control unit to said memory unit (i.e., bus between memory control unit 120 and memory hub 110 in Fig. 1) and comprising: a first signal line (i.e., signal line 150 of Fig. 2) formed on a first layer of said circuit board (e.g., surface layer on said circuit board) and connected to said memory control unit and to a first pin on said memory unit (See page 2, lines 3-8; i.e., connection between a pin 155 of Fig. 2 on memory unit 110 of Fig. 1 and memory control unit 120 of Fig. 1); and a second signal line (i.e., signal line 160 of Fig. 2) formed on said first layer (e.g., said surface layer on said circuit board) of said circuit board and also connected to said first pin connection on said memory unit (See page 2, lines 8-10), a first portion of said second signal line (i.e., "neck down" portion of signal line 160 of Fig. 2) at an acute angle (i.e., angle between neck down portions of the first and second signal lines in Fig. 2) relative to a first portion of said first signal line (i.e., "neck down" portion of signal line 150 of Fig. 2).

AAPA does not teach said circuit board comprising a second portion of said second signal line substantially parallel to a second portion of said first signal line; at least two layers formed in parallel to a surface of said circuit board, wherein said width of said lines and a perpendicular distance separating said second portions of said lines are each substantially equal, and wherein said first layer defines a non-grounded gap between said first and second portions of said first and second signal lines.

Perino discloses a circuit board (i.e., motherboard 110 of Fig. 1) comprising a second portion of a second signal line (e.g., a second half of trace 870 of Fig. 8, Example B) substantially parallel to a second portion of a first signal line (e.g., a second half of trace 880 of Fig. 8, Example B) with having substantially equal widths of said signal lines, and a distance (i.e., space) between said signal lines (i.e., 8 mils signal line in Fig. 8, Example B); at least two layers (e.g., signal traces' plane and a ground plane) formed in parallel to a surface (i.e., surface for the signal traces and pad contacts 1420 of Fig. 14) of said circuit board (See col. 4, lines 62-67), wherein said width (i.e., 8 mils signal line in Fig. 8, Example B) of said lines (i.e., the

portion of trace 870 and the portion of trace 880 in Fig. 8, Example B; Perino) and a perpendicular distance (i.e., a right angle distance with two signal lines, such as the shortest distance, 8 mils space in Fig. 8, Example B) separating said second portions of said lines are each substantially equal (i.e., 8 mils in Fig. 8, Example B), and wherein a layer (i.e., surface layer of motherboard 110 of Fig. 1) defines a non-grounded gap between a first portion and second portion of said first and second signal lines (i.e., a first and second half of respective traces 870 and 880 in Fig. 8, Example B; See Figs. 8 and 16, See col. 4, lines 66-67 and col. 7, lines 21-26; i.e., wherein in fact that a ground plane is on the backside of the motherboard, and those figures implies that a ground gap is not between said first portion and second portion of said first and second signal lines).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have motivated to employ the concept of the line width and space determination, as disclosed by Perino, to said circuit board routing, as disclosed by AAPA, so as to make (1) a second portion of said first signal line and a second portion of said second signal line route with a separating distance, and (2) said signal line widths of said first and second signal lines are equal to the width of said separating distance for the determined impedance values, for the advantage of eliminating reflected signals and signal deterioration caused by a mismatched impedance (See Perino, col. 5 lines 29-32).

Referring to claim 23, AAPA teaches said memory unit comprises a memory repeater hub (See page 1, line 12; i.e., memory hub 110 of Fig. 1).

Referring to claim 24, AAPA teaches said memory unit comprises a memory repeater hub (See page 1, line 12; i.e., memory hub 110 of Fig. 1).

Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Perino [US 6,160,716 A] as applied to claims 1, 4-8, 11-14, 16-20, 23 and 24 above, and further in view of Theus [US 4,904,968].

Referring to claim 3, AAPA, as modified by Perino, discloses all the limitations of the claim 3 except that does not teach third and fourth signal lines, on a second layer of said circuit board, different than said first layer.

Theus discloses a circuit board configuration for reducing signal distortion, wherein third and fourth signal lines (e.g., signal traces 26 and 32 in Fig. 4), on a second layer (e.g., signal layer 30 of Fig. 4) of said circuit board, different than a first layer (e.g., signal layer 20 of Fig. 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used said multiple layered circuit board, as disclosed by Theus, for said circuit board, as disclosed by AAPA, as modified by Perino, for the advantage of providing an improved circuit board for reducing signal distortion characteristics (See Theus, col. 4, lines 6-8).

Referring to claim 10, AAPA, as modified by Perino, discloses all the limitations of the claim 10, including portions of said first and second signal lines (i.e., a first and second half of respective traces 870 and 880 in Fig. 8, Example B) that are not separated by any conductive traces (See Perino, Figs. 8 and 16, i.e., no conductor line between traces 870 and 880 in Fig. 8 for maintaining the same width and space) except that does not teach another parallel layer of said circuit board over said portions of said first and second signal lines.

Theus discloses a circuit board configuration for reducing signal distortion, wherein third and fourth signal lines (e.g., signal traces 26 and 32 in Fig. 4), on another parallel layer (e.g., signal layer 30 of Fig. 4) of a circuit board (i.e., circuit board 10 of Fig. 4) over portions of first and second signal lines (i.e., traces on a surface of circuit board 10 in Fig. 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used said multiple layered circuit board, as disclosed by Theus, for said circuit board, as disclosed by AAPA, as modified by Perino, for the advantage of providing an improved circuit board for reducing signal distortion characteristics (See Theus, col. 4, lines 6-8).

(11) Response to Argument

Appellant's arguments with respect to Claim Group I (i.e., claims 1, 3-8, 10-14, 16-20, 23 and 24) have been considered.

In response to the Appellant's arguments with respect to Perino expressly teaches away from the claimed connection of signal lines on the Appeal Brief, page 6, line 10 through page 8, line 7, the Examiner believes that the Appellant misinterprets the claim rejection.

First of all, the Appellant essentially argues that Perino doesn't teach connecting signal lines to the same pin. However, AAPA teaches said signal lines (i.e., signal lines 150 and 160 in Fig. 2) being connected to the same pin (i.e., pin 155 of Fig. 2; See (10) Grounds of Rejection of the instant Examiner's Answer, claims 1, 4-8, 11-14, 16-20, 23 and 24 rejection under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Perino).

In succession, the Appellant argues that the claim rejection contends that one of ordinary skill would be motivated, not only to ignore the express teachings of Perino away from characteristics of the claimed invention, but also to pick and choose some particular characteristics of Perino's signal lines while discarding others to arrive at the claimed invention. In other words, the Appellant essentially argues that the Examiner contends that one of ordinary skill would do so for the advantage of eliminating reflected signals and signal deterioration caused by a mismatched impedance in contrary to Perino's description, such that achieving the cited elimination of reflected signals and mismatched impedance by maximizing the width of traces to reduce the impedance of those traces.

In fact, the cited background of Perino (See Fig. 8) discloses two examples (Example A and Example B) of signal line routing for achieving the cited elimination of reflected signals and mismatched impedance at col. 5, lines 1-41. And, the Appellant asserts as if the Example A, i.e., maximizing the width of traces to reduce the impedance of those traces, is the only way to achieve the asserted advantage of the cited background of Perino, i.e., eliminating reflected signals and signal deterioration caused by a mismatched impedance, but the Example B is also the other way to achieve the same asserted advantage of the cited background of Perino in case of having a given limited routing condition, e.g., a limited routing space between interfering objects on PCB.

Therefore, in contrary to the Appellant's statement, the purported motivation relied on in the claim rejection is relevant to the combination of AAPA and Perino, i.e., achieving the asserted advantage of the cited background of Perino (Example B), eliminating reflected signals and signal deterioration caused by a mismatched impedance, one of ordinary skill would follow the teaching of the cited prior art of Perino (Example B), such that two signal lines (i.e., traces 870 and 880 in Fig. 8), and space between said two signal lines being equal (See Perino, col. 5, lines 35-37).

Thus, the Appellant's argument on this point is not persuasive.

In response to the Appellant's arguments with respect to Perino teaches away from a non-ground gap between signal lines on the Appeal Brief, page 8, line 8 through page 10, line 5, the Examiner respectfully disagrees.

In contrary to the Appellant's statement, the claim rejection under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Perino, is not depending on the embodiment Fig. 11 of Perino. Instead, it depends on the embodiment Fig. 8 of Perino, which is not Perino's invention, but a background disclosed by Perino as a prior art. And, said geometry of said signal lines in the background (Fig. 8 Prior Art) shows an advantage of eliminating reflected signals and signal deterioration caused by a mismatched impedance

eliminating reflected signals and signal deterioration caused by a mismatched impedance by way of minimizing the distance between traces, while maximizing the width of the traces, as exemplified by Example A in Fig. 8, and also the other way, such that the routing geometry in the claimed invention, i.e., substantially parallel signal lines, their line widths and a perpendicular distance separating said lines being each substantially equal (i.e., no conductive lines between said signal lines including a ground connection), to achieve the same asserted advantage of the cited prior art of Perino in case of having a given limited routing condition, e.g., a limited routing space between interfering objects on PCB, as exemplified by Example B in Fig. 8. (Refer to col. 5 lines 19-41).

Furthermore, the Appellant asserts as if Perino teaches that the gap between the traces should be grounded, and then successively argues the claim rejection ignores this teaching, i.e., a ground trace between signal traces (See the Appeal Brief, page 8, lines 10-21).

However, Perino suggests to the artisan to place, or not to place a ground gap between signal lines (i.e., signal traces) based upon the need for signal isolation between said signal lines, i.e., (1) placement of large spacing without needing said ground gap, (2) providing said ground gap between said signal lines for preventing signal interferences, or (3) said ground gap may be selectively used between said signal lines that may cause interferences (See col. 5, line 56-58, col. 6, lines 14-17 and 36-38). In fact, AAPA teaches said signal lines are connected at a first pin (i.e., constructing one single connection line), thus the artisan does not place said ground gap (i.e., ground tracer) between said signal lines according to Perino's clear suggestion because said signal lines (i.e., one single connection line) doesn't cause any interferences (See col. 6, lines 36-38 about said ground gap may be selectively used between said signal lines that may cause interferences). Moreover, Perino provides another clear teaching that the gap between the traces may not be grounded because the opposite side of board provides the ground connection (See Perino, col. 7 lines 48-50; i.e., Perino doesn't teach the gap between the traces should be grounded, but the gap

between the traces may be grounded or may not be grounded depending on the routing condition on the board).

In succession, the Appellant alleges that Perino's teachings regarding the **undesirability** of a non-grounded gap are relevant to the present patentability determination (See the Appeal Brief, page 9, lines 6-19). However, Perino **never teaches/suggests** that said non-grounded gap between signal traces is **undesirable**. Instead, Perino shows not only a board may selectively include isolating trace between said signal traces for preventing signal interferences in Fig. 11, illustrated as an embodiment, but also a board may exclude isolating trace between said signal traces in Fig. 16, illustrated as another embodiment. Thus, the Appellant's argument on this point is not persuasive.

In response to the Appellant's arguments with respect to There is no suggestion to combine and/or a reasonable expectation of success founded in the prior art on the Appeal Brief, page 10, line 6 through page 12, line 28, the Examiner respectfully disagrees.

As the Examiner has already discussed in the above argument responses, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Moreover, in response to the Appellant's argument that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the Appellant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Especially, the Appellant asserts as if Perino disparages "two-between routing", and argues that the claim rejection relied upon the embodiment of Fig. 8 is disadvantageous on the Appeal Brief, page 12, lines 4-9. In contrary to the Appellant's statement, Perino points out "two-between routing **may** (i.e., not all the time) cause interference between the signals carried by wither of the traces", and "thin traces have an increased impedance, that does not match the impedance of the signals" at col. 2, lines 15-33, then describes solutions by two examples in case of causing interference from two-between routing, such that (1) Example A in Fig. 8, by way of minimizing the distance between traces, while maximizing the width of the traces, and (2) Example B in Fig. 8, substantially parallel signal lines, their line widths and a perpendicular distance separating said lines being each substantially equal under a given limited routing condition, e.g., a limited routing space between interfering objects on PCB. And, Perino continuously describes the advantage of the solutions, i.e., eliminating reflected signals and signal deterioration caused by a mismatched impedance. And, the Examiner has clearly pointed out rationale for appropriate combination of the references based on the above motivation.

Thus, the Appellant's argument on this point is not persuasive.

Appellant's arguments with respect to Claim Group II (i.e., claims 8 and 10-13) have been considered.

In response to the Appellant's arguments with respect to CLAIM 8 on the Appeal Brief, page 13, the Examiner respectfully disagrees.

In contrary to the Appellant's statement, the method steps of claim 8 are performed by means for function, which are drawn from the apparatus of claim 1 as follows.

As the Examiner shows the obviousness of the claimed invention in the claim rejection (See (10) Grounds of Rejection of the instant Examiner's Answer, claims 8 rejection under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Perino), ① a method step for delivering a first signal over a first signal line on a first layer formed in parallel to a second layer on a surface of a multi-layer circuit board

and connected between a memory control unit and a first pin on a memory unit *is performed by* a circuit board comprising at least two layers formed in parallel to a surface of said circuit board, a first signal line, formed on a first layer of said circuit board and connected between a first pin on a memory unit and a memory control unit, which is taught by AAPA in view of Perino in the claim 1; ② a method step for delivering a second signal over a second signal line formed on said first layer of said circuit board and connected to said first pin on said memory unit, a first portion of said second signal line formed at an acute angle relative to a first portion of said first signal line, a second portion of said second signal line formed substantially parallel to a second portion of said first signal line, said first and second portions of said first and second signal lines separated without a ground connection therebetween *is performed by* said circuit board comprising a second signal line also formed on said first layer of said circuit board and connected to said first pin on said memory unit, a first portion of said second signal line at an acute angle relative to a first portion of said first signal line, a second portion of said second signal line formed substantially parallel to a second portion of said first signal line, wherein said first layer defines a non-ground gap between said first and second portions of said first and second lines, which is taught by AAPA in view of Perino in the claim 1.

Thus, the Appellant's argument on this point is not persuasive.

Appellant's arguments with respect to Claim Group III (i.e., claims 14 and 16-19) have been considered.

In response to the Appellant's arguments with respect to CLAIM 14 on the Appeal Brief, page 14, the Examiner respectfully disagrees.

In contrary to the Appellant's statement, the method steps of claim 14 should have been performed by means for manufacturing, which are inherently drawn from the apparatus of claim 1 as follows.

As the Examiner shows the obviousness of the claimed invention in the claim 14 rejection (See (10) Grounds of Rejection of the instant Examiner's Answer, claims 14 rejection under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Perino), ① a method step for forming at least two layers parallel to a surface of a circuit board, with first and second signal lines on a first layer of said board *is inherently drawn from* a circuit board comprising at least two layers formed in parallel to a surface of said circuit board, a first signal line, formed on a first layer of said circuit board, and a second signal line also, formed on said first layer of said circuit board, which is taught by AAPA in view of Perino in the claim 1; ② a method step for connecting a memory unit to said board such that a first pin on said memory unit connects to said first and second signal lines *is inherently drawn from* said second signal line on said circuit board being connected to a first pin on said memory unit, which is taught by AAPA in view of Perino in the claim 1; ③ a method step for affixing a memory control unit to said board such that said memory control unit connects to at least said first signal line *is inherently drawn from* said first signal line on said circuit board being connected between said first pin on said memory unit and a memory control unit, which is taught by AAPA in view of Perino in the claim 1; ④ a method step for forming a first portion of said second signal line to be at an acute angle relative to a first portion of said first signal line *is inherently drawn from* said circuit board further comprising a first portion of said second signal line at an acute angle relative to a first portion of said first signal line; ⑤ a method step for forming a second portion of said second signal line to be substantially parallel to a second portion of said first signal line *is inherently drawn from* a second portion of said second signal line formed substantially parallel to a second portion of said first signal line, which is taught by AAPA in view of Perino in the claim 1. Thus, the Appellant's argument on this point is not persuasive.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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